MEMORY CELLS ENHANCED FOR RESISTANCE TO SINGLE EVENT UPSET

ABSTRACT

Method and apparatus are described for providing memory cells enhanced for resistance to single event upsets. In one embodiment, transistors are coupled between cross coupled inverters of a latch, thus in a small area providing both single-event-upset resistivity most of the time, and high speed during writing to the memory cell. Alternatively, inductors coupled between inverters of a latch may be used.